IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY, Plaintiff, v. STMICROELECTRONICS INTERNATIONAL N.V., and STMICROELECTRONICS, INC, Defendants.	CIVIL ACTION NO. 6:21-CV-00727-ADA JURY TRIAL DEMANDED

PLAINTIFF'S RESPONSE TO DEFENDANTS' MOTION FOR PARTIAL SUMMARY JUDGMENT THAT CLAIM 10 IS INDEFINITE

TABLE OF CONTENTS

TABLE OF AUTHORITIES

CASES:

I. Introduction

Plaintiff, the Trustees of Purdue University ("Purdue"), respectfully submits its response to Defendants' Motion for Partial Summary Judgment That Claim 10 is Indefinite. For the same reasons that claim 9's use of "less than about three micrometers" is not indefinite, claim 10's use of "about one micrometer" is not indefinite. Defendants incorrectly argue that the patent does not explain the "purpose" of having a JFET width of "about one micrometer." The specification's guidance includes optimizing the width of the JFET region to achieve two aims of the invention, increased blocking voltage and reduced on-resistance. Given these goals and reading these teachings, a skilled artisan would focus on keeping the JFET region width as narrow as possible. Under the patent, widths of "about three micrometers" and "about one micrometer" meet this goal. Further, the Court rightly considered and measured the evidence regarding variation in fabrication of the claimed devices. Finally, a person of ordinary skill would readily understand how and where to measure the claimed JFET width given the plain terms of the specification and basic semiconductor fundamentals. Defendants have not met their clear and convincing burden to show that claim 10 is indefinite.

II. Related Materials and Disputed Facts

Purdue affirmatively has sought a determination that claim 10 is not indefinite. *See* Dkt. 360 at 13-17. Purdue incorporates by reference in full its briefing and exhibits from its own motion. Exhibit 6 to Purdue's motion is the August 7, 2023 Memorandum Opinion and Order of Judge Osteen in the related case *The Trustees of Purdue University v. Wolfspeed, Inc.*, pending in the U.S. District Court for the Middle District of North Carolina. Judge Osteen found that claim 10 was not indefinite, rejecting many of the same arguments that Defendants make here. Purdue reattaches Judge Osteen's Order as Exhibit 1 to this brief.

Further, Purdue disputes certain purported "Undisputed Material Facts" in Defendants' Motion. First, Purdue disputes ¶ 3 that the specification does not disclose the purpose of the claimed JFET width. That is incorrect. As discussed below, the specification details the goals of a narrow JFET width, especially as it relates to on-state resistance and breakdown voltage.

Second, Purdue disputes ¶ 5 because there is no support for Defendants' allegations in that paragraph. Dr. Neikirk's deposition testimony does not support the proposition in ¶ 5 that the "amount of variation would not simply scale up or down when larger or smaller features are fabricated." Indeed, Defendants do not submit any expert testimony regarding indefiniteness of claim 10. Some courts have held that a defendant's failure to provide expert testimony regarding indefiniteness is fatal to the argument. *See Apple v. Samsung Elecs. Co., Ltd*., 786 F.3d 983 (Fed. Cir 2015), *rev'd and remanded on other grounds*, 137 S. Ct. 429 (2016) (affirming decision rejecting indefiniteness because Samsung offered "no evidence showing that skilled artisans would find the element 'substantially centered' as lacking reasonable certainty in scope"); *Lecat's Ventriloscope v. MT Tool and Manufacturing*, 351 F.Supp.3d 1100, 1114 (N.D. Ill. 2018) (denying indefiniteness challenges because accused infringer "has no expert to testify as to the indefiniteness of this term" and "[w]ithout any affirmative testimony, Defendant will be unable to offer the perspective of a POSITA").

Purdue disputes ¶ 6 to the extent that Defendants posit that a skilled artisan would not understand "the particular equipment or processes to be used for fabricating the claimed devices or the inherent manufacturing tolerances associated with the particular equipment or processes to be used." In *Source Search Technologies, LLC v. LendingTree, LLC*, 588 F.3d 1063, 1077 (Fed. Cir. 2009), the Federal Circuit rejected the notion that a skilled artisan would read the text of the claim language without bringing to bear her knowledge and expertise. The Court reiterated, "this court

measures indefiniteness according to an objective measure that recognizes artisans of ordinary skill are not mindless 'automatons.'" *Id*. (quotations omitted).

III. Legal Standard

In *Nautilus, Inc. v. Biosig Instruments*, 134 S. Ct. 2120, 2124, 2128-30 (2014), the Supreme Court held that "a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." The Supreme Court added that while the definiteness requirement "mandates clarity, while recognizing that absolute precision is unattainable." *Id*. Defendants must establish indefiniteness by clear and convincing evidence. *BASF Corporation v. Johnson Matthey Inc*., 875 F.3d 1360, 1365 (Fed. Cir. 2017). Defendants have not and cannot meet their burden.

IV. Argument

A. The Specification Discloses the Purpose of the JFET Region

The use of "about" does not render claim 10 indefinite. As this Court previously found, "terms of approximation like 'about' or 'at least about' are common in patent law and the Federal Circuit has confirmed that they are not indefinite." Dkt. 220 at 30 (citing *Merck & Co. v. Teva Pharms. USA, Inc*., 395 F.3d 1364, 1369 (Fed. Cir. 2005). The Court likewise previously found "that a POSITA would understand that 'about' is not indefinite, but rather, at minimum, was intended to account for well-known fabrication variation." *Id*.

Despite this prior rejection of their arguments, Defendants recycle arguments and attempt to show indefiniteness by arguing that "neither the intrinsic record nor extrinsic record explain the JFET width's purpose." Motion at 4. Defendants unsuccessfully made a nearly identical argument as to claim 9. Dkt. 220 at 27-28. Yet again, Defendants' argument does not pass muster because the specification, as read by a skilled artisan, repeatedly discusses the purpose of the JFET width. And in

making their arguments, Defendants manufacture phantom requirements that the claim language must meet without identifying any authority for their arguments.

The background of the invention identifies two design considerations of high-voltage power MOSFETs: "blocking voltage" and "specific on-resistance." *Id*. at 1:18-35. The specification defines blocking voltage as the drain-to-source voltage of the device "at which avalanche breakdown occurs and/or the strength of the magnetic field of the gate oxide at which the gate oxide fails." *Id*. at 1:21-25. The specific on-resistance of a semiconductor device is the "product of the resistance of the device between the source and drain when the device is in an on-state and the area of the device." *Id.* at 1:28-31. The specification also explains that "[a]s the specific on-resistance of the device decreases, the efficiency of the semiconductor device may be improved," but "the typical fabrication techniques for reducing specific on-resistance of high-power semiconductor devices may also reduce the blocking voltage of the device." *Id*. at 1:31-36. The specification explains that a JFET region with a narrow width, such as the claimed less than about three microns, "may reduce the specific on-resistance of the semiconductor device." *Id*. at 6:22-24. Likewise, this narrow JFET region allows for increased blocking voltage "because such a configuration may reduce the magnetic field in the gate oxide layer above the JFET region 30." *Id*. at 6:48-50.

Purdue's claim construction expert, Dr. Shanfield, opines on how the width of the JFET region relates to the purpose of the invention:

> Because the goal of the device design is to achieve the lowest possible on-resistance while meeting the desired blocking voltage specification ('633 Patent at 1:18-36), a POSITA would understand that a JFET region that was too wide would result in the field across the gate oxide in the blocking state to exceed the electric field for oxide breakdown, thus damaging the gate oxide. … On the other hand, a JFET region that was too narrow would increase the on-state resistance, contrary to the design goal. Therefore, there is an optimum width at which one achieves the lowest on-resistance without allowing the oxide field to exceed the electric field for oxide breakdown in the blocking state.

Ex. 2 (Shanfield Report) at ¶ 46.[1] This Court similarly cited the specification's "design guidance and objectives including optimizing the width to reduce the on-resistance and the electric field, and ensuring good forward current conduction and withstanding reverse blocking voltage." Dkt. 220 at 30-31 (citing '633 Patent at 1:18-36). And in finding claim 10 not indefinite, Judge Osteen likewise noted that the function of the JFET width is "to optimize between a lower on-resistance and desired blocking voltage" and that a "person skilled in the art could test the on-resistance and blocking voltage to ensure that the two are optimized to serve the purpose of the MOSFET device." Ex. 1 at 36. The foregoing intrinsic and extrinsic evidence explains the JFET width's purpose, *i.e.*, to provide sufficiently desired, or optimal, on-resistance and blocking voltage parameters. Claim 10 states that one such width is about one micrometer.

Defendants argue that this is insufficient because the specification "does not say there is any particular characteristic or purpose of the device that is achieved with a JFET width in the vicinity of about 1 micrometer that is not achievable at other dimensions—whether 0.9 micrometers, 1.1 micrometers, 1.3 micrometers, or any other dimension." Motion at 4. This argument effectively negates the claim language. Claim 10 reflects that the inventors' view that a JFET width of "about one micrometer" achieves the goals of the invention stated in the specification (and reinforced by the extrinsic record). The inventors did not just contemplate "any other dimension." And they used "about" to account for well-recognized manufacturing and fabrication variations. *See* Dkt. 220 at 30; Ex. 2 (Shanfield Report) at ¶¶ 43-44, 50. Contrary to Defendants' suggestion, the inventors did not have to go through all possible JFET widths and explain whether they met the goals of the invention.

[1] Dr. Shanfield's report from the *Wolfspeed* case is also attached as Exhibit 7 to Purdue's affirmative motion, Dkt. 360.

Defendants also argue that the specification does not disclose any result or purpose that is achieved by "'about one micrometer' that is different than 'less than about three micrometers.'" Motion at 4. This is a strawman. The patent need not articulate a different result or purpose for JFET regions having a width of "about one micrometer," and Defendants do not cite any authority for the proposition that two claimed widths must achieve different results. A skilled artisan reading the specification would understand that the results can be the same, *i.e.*, reduction of on-state resistance with a desired blocking voltage, for two different JFET widths—the specification does not teach different goals based on various widths.

Defendants next argue that "neither the desired on-resistance nor desired blocking voltage are specified by the claim or the specification." Motion at 5. This argument overlooks the specification's repeated goal of obtaining as low an on-resistance as possible while maintaining a sufficient blocking voltage. Those two competing goals do not have to be numerically defined in a patent claim for a skilled artisan to appreciate them and thereby understand how the claimed invention's various JFET widths can be used with almost limitless combinations of doping types and concentrations depending on the application's specification as to on-resistance and blocking voltage. Ultimately, Defendants' argument that "there is no basis in the specification from which to determine the criticality of the 'about one micrometer' JFET width" is simply incorrect. It certainly does not prove indefiniteness by clear and convincing evidence.

B. <u>The Court Properly Relied on the Record Before It</u>

Defendants argue that it was improper for the Court to rely on extrinsic evidence from Plaintiff's claim construction expert, Dr. Bhat, regarding the amount of variation. Motion at 5. Defendants appear to agree that such variation exists but dispute the nature and extent of such

variation.[2] In their motion, however, Defendants do not offer any competing expert opinions on the amount of fabrication variation. Instead, Defendants attack Dr. Bhat's reliance on a textbook in support for the view that +/- 10% variation is expected, arguing that such variation leads to absurd results. *Id*. at 6.

Defendants' argument confirms that claim 10 is not indefinite. If a skilled artisan understands that a one micrometer feature can vary in width by 0.1 micrometers (or about 10%), then claim 10 cannot be indefinite. What Defendants are trying to do is show that a three-micrometer feature cannot vary by 0.3 micrometers—essentially a backdoor motion for reconsideration. But there is no support for Defendants' extrapolation. Simply because a one micrometer device might have a narrower variance does not *ipso facto* mean that a larger device must have the same variance. A larger device may have a broader variance because of the methods or equipment of manufacture. The textbook cited by Defendants does not speak to the three-micrometer scenario. To the contrary, the textbook contemplates various linewidths. Dkt. 76-2 at 6.

Defendants' argument that a POSITA would need to know the equipment and processes used to understand the tolerances, Motion at 6, likewise goes too far. A skilled artisan would understand the techniques of manufacturing the claimed silicon carbide device, including the equipment involved. For example, a skilled artisan would understand that diffusion cannot be performed on silicon carbide. *See* Ex. 3 (Cooper Dep. Tr.) at 310:21-311:8. Again, contrary to Defendants' view, the skilled artisan is not a mindless automaton.

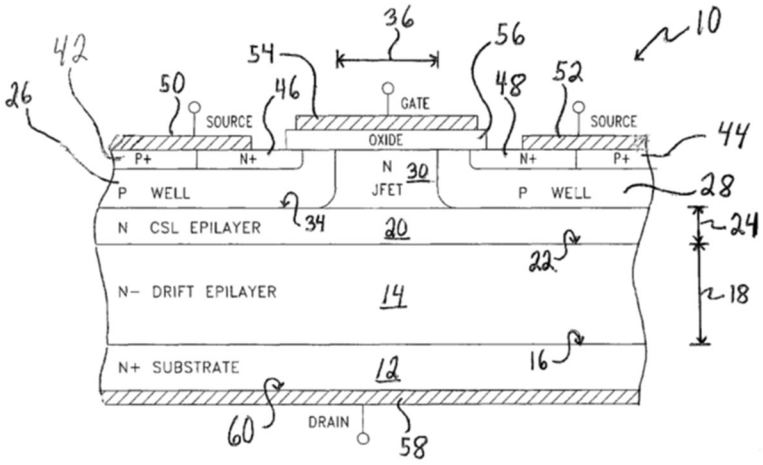
Defendants also argue that nothing in the intrinsic evidence that even suggests that "about" is intended to address manufacturing tolerances. Motion at 7. The Court rightly rejected this same

[2] Defendants' non-infringement expert, Dr. Neikirk, admits that variation would occur. *See* Ex. 4 (Neikirk Report) at ¶¶ 154-156. Their invalidity expert, Dr. Lipkin, agrees. *See* Ex. 5(Lipkin Report) at ¶ 859.

argument when lodged against claim 9. Dkt. 220 at 27-28. The use of the word "about" itself is intended to mean "approximately." And it is common knowledge—as reflected in the textbook cited by Defendants—in the field that there is variation in semiconductor fabrication as in other types of manufacturing. *Id*. at 30 ("[A] POSITA would understand that semiconductor fabrication is not an absolutely precise process, but like other manufacturing processes, there are small variations.").

C. A Skilled Artisan Would Know Where to Measure

Defendants argue that the "specification and claims of the '633 Patent also do not inform a POSITA where or how the width of the JFET region should be measured relative to the boundary of the P wells or source regions." Motion at 7. This is demonstrably false. The specification shows that while the JFET region lies between the P wells, the width of the JFET region is measured between the vertical edges of the P wells. Figure 1 of the specification is all but dispositive. Figure 1 shows that the JFET width (designated as item "36") is the width between the vertical edges of the P wells, *i.e.*, its narrowest width, and the specification explains: "For example, in some embodiments, the JFET region 30 has a width 36 that is about three micrometers or less. In one particular embodiment, the JFET region 30 has a width 36 of about one micrometer." '633 Patent at 6:24-27; *see also id.* at 6:45-50 ("Conversely, the shorter width 36 of the JFET region 30 compared to typical semiconductor device may tend to increase the blocking voltage of the semiconductor device 10 because such a configuration may reduce the magnetic field in the gate oxide layer above the JFET region 30.").



Nothing in the specification suggests that the JFET width may be measured at the curved portions of the P wells and nothing in the specification states that the curved portions of the P well factor into determination of the JFET width. Had the inventors contemplated that the JFET width implicates the curved portions, they would have showed as much in Figure 1 or said as much in the specification. They did not. The inventors explicitly told the public that the JFET width is measured between the P wells at their vertical edges, *i.e.*, the narrowest point between the P wells.

The JFET width as described in the specification is consistent with the technological reality of current flow. Any width other than the width between the vertical edges of the P wells, *i.e.*, the narrowest width, is immaterial to the relevant semiconductor parameters, such as on-state resistance. Any width other than the narrowest would not be indicative of the device's resistance and would not provide an accurate measurement for purposes of breakdown voltage. Consider a narrowing water pipe (or funnel) analogy: the rate of flow of the water is limited by the narrowest section of the pipe regardless of the larger width of the stages of the pipe at either end.

Another helpful semiconductor analogy is an hourglass. When the device is "on," sand (current) flows from the upper half (source) to the lower half (drain). The width of the hourglass's neck *at its narrowest distance* (the JFET region width) controls the rate at which sand (current) passes from one half to the other.

Changing the location of the narrowest point as indicated in the following graphics, *i.e.*, lower in the neck (left graphic) or upper in the neck (right graphic), does not change the fact that the narrowest distance dictates the rate of flow.

The curvature of the flared regions outside the pinch point is immaterial.

Similarly, the narrowest point between the P wells is the rate-limiting section of the claimed MOSFET for purposes of current travel. Current cannot pass at any other point. Accordingly, when skilled artisans speak of on-resistance, for example, it is necessarily the resistance measured at the area through which current passes, *i.e.*, the narrowest width between the P wells. Any other measurement would not accurately reflect the on-resistance or the electrical properties of the device.

Defendants try to dismiss Figure 1 and its accompanying description, arguing that it does not address that the edges of the P wells are curved or that the patent figure is not drawn to scale. Motion at 7-8. The possibility of the curvature of the P wells affecting the measurement of the

JFET width is, as discussed above, specifically contemplated by the specification, which teaches that P well curvature is not part of the JFET width. The specification clearly shows that the linear portions of the P well boundaries delineate the JFET width (36), as the inventors intended. Defendants conflate the specification's teaching of the JFET region with its teachings of the JFET width. While Figure 1 shows that the JFET region (30) may include curved portions under the P wells, the specification and Figure 1 define the width of the JFET to be (36), which excludes the curved portions and shows the JFET width to be measure at the narrowest point between the P wells.

Defendants' "not to scale" argument is even more unavailing. Scale has nothing to do with where and how Figure 1 was annotated and what JFET width **(36)** excludes. That Defendants do not (and cannot) argue that the JFET width **(36)** includes the curved regions speaks volumes. Defendants cannot meet their burden to invalidate a patent by clear and convincing evidence merely by arguing that a figure, which intentionally excludes the curved portion from the JFET width, is not drawn to scale.

Defendants also argue that the alleged ambiguity of claims is "compounded by different definitions of in the specification and claims" and that both the P well region and the source regions have curved sides. Motion at 8. This is another strawman. As discussed at length in Purdue's Motion for Supplemental Claim Construction, the JFET region is the region between the P wells, which is also located between the first and second source regions. Dkt. 360 at 4-11. Any curvature of the source regions is thus irrelevant given that the source regions do not provide the boundaries of the JFET region and thus are not implicated in determining the JFET width.[3]

[3] Judge Osteen rejected similar attempts to foment ambiguity where there is none. In his August 7, 2023 Opinion and Order, he rejected Wolfspeed's argument that the alleged "inconsistency between the claim term and the specification means that the width of the JFET region will vary depending on

Finally, Defendants argue that Purdue has vacillated in its interpretation and assertion of the claim language. Motion at 9. Not so. As Defendants themselves argue, Purdue has taken the position that +/- 10% variance is acceptable. Dr. Cooper's opinions are consistent with that variance. His addition of "or so" does not change that nor does it prove by clear and convincing evidence that claim 10 is indefinite.

V. Conclusion

Defendants have not met their burden to show that Claim 10 is indefinite, and their Motion should be denied for the foregoing reasons and for the reasons set forth in Purdue's Motion (Dkt. 360).

Dated: August 22, 2023

Respectfully submitted,

By: */s/John P. Lahad*

Michael W. Shore (SBN 18294915)
Chijioke E. Offor (SBN 24065840)
Halima Shukri Ndai (SBN 24105486)
THE SHORE FIRM LLP
901 Main Street, Suite 3300
Dallas, Texas 75202
Telephone: (214) 593-9110
Fax: (214) 593-9111
mshore@shorefirm.com
coffor@shorefirm.com
hndai@shorefirm.com

---

the boundaries from which it is measured." *See* Ex. 1 at 22. He ruled that "there is no inconsistency between the claim term and the specification rendering the claim term indefinite" and that the "claims term, specification and Figure 1 taken together demonstrate the JFET region falls between both the source regions and the p-wells." *Id*. at 28; *see also id.* ("the JFET region must fall between the p-wells, as well as the first and second source regions").

Brian D. Melton (SBN 24068095)
John P. Lahad (SBN 24068095)
Abbey McNaughton (SBN 24116751)
SUSMAN GODFREY L.L.P.
1000 Louisiana Street, Suite 5100
Houston, Texas 77002
Tel: (713) 651-9366
Fax: (713) 654-6666
bmelton@susmangodfrey.com
jlahad@susmangodfrey.com
amcnaughton@susmangodfrey.com

COUNSEL FOR PLAINTIFF
THE TRUSTEES OF PURDUE UNIVERSITY

CERTIFICATE OF SERVICE

In accordance with Federal Rule of Civil Procedure 5 and Local Rule CV-5, I hereby certify that a true and correct copy of the foregoing has been served on counsel for Defendants VIA ECF and email on August 22, 2023.

/s/ John Lahad